What is claimed is:

1. A method for generating a set of test sequences for testing an integrated circuit, each test sequence of the set of test sequences containing a plurality of bits defining test inputs for the integrated circuit, the method comprising the steps of:

defining a list of faults for the integrated circuit;

generating at least one test sequence that defines values for those inputs necessary to detect at least one target fault selected from the list of faults, the values comprising only a portion of the bits of the at least one test sequence, wherein a remainder of the bits in the at least one test sequence are unspecified bit positions; and

setting the values of a plurality of the unspecified bit positions using a non-random filling methodology.

2. The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions to a value of one.

3. The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions to a value of zero.

4. The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes extending a value of a last specified bit position to set a plurality of the unspecified bit positions to a value equal to the last specified bit position.

5. The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions using a repeating pattern of ones and zeros.

6. The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions using an algorithm that is conducive to compression.

7. The method as defined in claim 1, further including the step of setting a plurality of the unspecified bit positions in accordance with a random filling methodology.

8. The method as defined in claim 1, further including the steps of:

adding a first test sequence to a list of test sequences and marking the selected fault as detected;

generating an additional test sequence which defines values for those inputs necessary to detected a target fault selected from the list of faults, and other than one marked as detected;

determining whether the additional test sequence may be compacted with any test sequence in the list of test sequences, and if so, compacting the additional test sequence with a test sequence in the set of test sequences, and if not, adding the additional test sequence to the set of test sequences.

9. The method as defined in claim 1, wherein a first test sequence of the plurality of test sequences defines values for those inputs necessary to detect a plurality of target faults selected from the list of faults.

10. The method as defined in claim 1, wherein additional test sequences of the plurality of test sequences define values for those inputs necessary to detect a plurality of target faults selected from the list of faults.

11. The method as defined in claim 1, wherein a first test sequence of the plurality of test sequences defines values for only those inputs necessary to detect a target fault selected from the list of faults.

12. The method as defined in claim 1, further including the step of fault simulating a first test sequence created in step (b) to determine if the first test

sequence detects additional faults, and if so, marking said additional faults as detected.

13. The method as defined in claim 1, wherein the integrated circuit is a portion of a larger integrated circuit chip.

14. The method as defined in claim 1, wherein outputs for the at least one test sequence are generated in response to the compacted condition.

15. An apparatus for generating a set of test sequences comprising:

first means for evaluating a list of faults and generating at least one test sequence configured to test at least one fault on the list of faults, the at least one test sequence defining values for those inputs necessary to detect at least one target fault selected from the list of faults, the values comprising only a portion of the bits of the at least one test sequence, wherein a remainder of the bits in the at least one test sequence are unspecified bit positions; and

second means for setting a plurality of the values of the unspecified bit positions using a non-random filling methodology.

16. The method as defined in claim 15, wherein the second means sets the values of the unspecified bit positions by setting each of the unspecified bit positions to a value of one.

17. The method as defined in claim 15, wherein the second means sets the values of the unspecified bit positions by setting each of the unspecified bit positions to a value of zero.

18. The method as defined in claim 15, wherein the second means sets the values of the unspecified bit positions by setting each of the unspecified bit positions to a repeating pattern of ones and zeros.

19. The method as defined in claim 15, wherein the step of setting the values of the unspecified bit positions includes extending a value of a last specified bit position to set a plurality of the unspecified bit positions to a value equal to the last specified bit position.

20. The method as defined in claim 15, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions using an algorithm that is conducive to compression.